

Abstract

5 A predetermined error vector magnitude reduction circuit exploits scatter
patterns that develop at the output of modern wireless communication systems
during phase state transition. Digital inphase and quadrature input signals to the
circuit, typically from a baseband processor, are compared to known characteristic
bit patterns that are pre-stored in a lookup table. Modified data that correspond to
10 the known characteristic bit patterns is supplied to the circuit to replace the data
signals themselves. The modified data may be digital data that replaces the digital
signals at the input to the inphase and quadrature DACs, or analog data that replaces
the analog output of the DACs.

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